



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/526,097	09/07/2005	Thomas Mueller	14603-012US1	2670

26161 7590 08/03/2009
FISH & RICHARDSON PC
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER

NATALINI, JEFF WILLIAM

ART UNIT	PAPER NUMBER
----------	--------------

2831

NOTIFICATION DATE	DELIVERY MODE
-------------------	---------------

08/03/2009

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No. 10/526,097	Applicant(s) MUELLER, THOMAS	
	Examiner JEFF NATALINI	Art Unit 2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 7/8/09 (IDS filed after RCE on 5/20/09).
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,5-8,10,12-15 and 17-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1,5-7,17 and 20-22 is/are allowed.
- 6) ☒ Claim(s) 8,10,12-15,18,19 and 23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 December 2008 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>7/8/09</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/20/09 has been entered.

Claim Rejections - 35 USC § 103

2. Claims 10, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kish et al. (7043109) in view of Kai et al. (US Publication 2002/0070359).

In regard to claims 10, 12, and 13, Kish et al. discloses a method (Fig. 17,23) for use with an integrated circuit (PIC) that is light-sensitive, illuminating different wavelengths (Fig. 33,34) of light 132 from external light source (laser)(column 21 line 62,63) to the integrated circuit, the integrated circuit comprising a photodiode (col 14 lines 11-15) producing output signals in response to the different wavelengths of light, measuring the output (column 21 line 63) signals to obtain measured values; comparing the measured values to setpoint values 140 (desired output) that correspond to the different wavelengths of light, obtaining correction values (calibrate data) for the different wavelengths of light, the correction values being based on comparison 140 of

Art Unit: 2831

the measured values to the setpoint value 140 (desired output) and also based on the sensitivity-power of the photodiode (col 16 lines 26-42) and storing (144,232) (Fig. 17,23) the correction values on the integrated circuit (column 34 lines 6-10), wherein the semiconductor chip comprise the integrated circuit (figure 22, IC- 10 is located inside the wafer-11), and discloses wherein the system includes a temperature monitor, wherein temperature and light intensity are both related to the wavelength (col 4 lines 44-49).

Kish et al. lacks specifically a temperature sensor for measuring temperature of light source and correction data derived from the temperature so that the output signal correcting information is based on the temperature of the external light source, so that it is on the integrated circuit.

Kai et al. discloses a temperature sensor that determines a temperature of the light sources, and uses the output of the temperature sensor to control the oscillation wavelengths by compensation for temperature conditions (abstract), temperature sensor (figure 3 element 24) is in the vicinity of the LD array chip-20 (chips are known to be located on integrated circuits/wafers- there would be a type of board/motherboard/integrated circuit supporting and providing proper connections- power and ground- to the chip and thermistor, possibly being shown in the figure by the unlabeled box surrounding elements 20 and 24).

At the time the invention was made it would have been obvious for one of ordinary skill in the art to modify Kish et al. by adding a temperature sensor (which would be obvious to be on the integrated circuit as the PIC has optic components-

Art Unit: 2831

abstract, and the temperature sensor would have the added functionality to make sure all the other chips on the integrated circuit and wafer don't overheat) for measuring the temperature of light source for correction of the wavelengths as taught by Kai et al., (during modification it would be known to be place on the integrated circuit of Kish et al., (similar to how Kai is described as an integrated circuit above) as the PIC -located on a wafer- has optic components-abstract- also the temperature sensor would provide the added functionality to make sure all the other chips on the integrated circuit and wafer don't overheat) in order to be able to easily control the wavelength in the system (page 1 paragraph 10).

In regard to claim 14, Kish et al. discloses wherein the integrated circuit is on a semiconductor substrate 32 (Fig. 6).

In regard to claim 15, Kish et al. discloses wherein the integrated circuit comprises one or more photodiodes able to receive different wavelengths of light PD (Fig. 37).

3. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kish et al. (7043109) and Kai et al. (US Publication 2002/0070359) as applied to claim 10 above, and further in view of Schmeizer (US Publication 2002/0048022).

In regard to claim 19, Kish et al. as modified discloses wherein the integrated circuit (PIC) has a sensitivity that is wavelength dependent (i.e. the integrated circuit is sensitive to different wavelengths of laser).

Art Unit: 2831

Kish et al. as modified lacks wherein the measured values define a sensitivity curve, wherein a smallest interval between two of the different wavelengths on the sensitivity curve is smaller than an interval between a relative maximum and a relative minimum on the sensitivity curve, in part, by the two measured wavelengths.

Schmeizer et al. discloses a sensitivity curve (figure 2) based on measured values of wavelengths from LEDs or lasers (page 3 paragraph 21), wherein a smallest interval between two of the different wavelengths on the sensitivity curve is smaller than an interval between a relative maximum and a relative minimum on the sensitivity curve (figure 2, many samples are taken so intervals between wavelengths are small).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Kish et al. as modified to include a sensitivity curve using with many measurements, so that a smallest interval between two of the different wavelengths on the sensitivity curve is smaller than an interval between a relative maximum and a relative minimum on the sensitivity curve, as taught by Schmeizer et al. in order to measure the quality of dispersion or distribution of the measured values in a matrix (page 1 paragraph 4).

4. Claims 8, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kish et al. (7043109) in view of Kai et al. (US Publication 2002/0070359) and D'Angelo (6621284).

In regard to claim 8, Kish et al. discloses a semiconductor chip (figure 22-PIC is part of semiconductor chip) comprising: an integrated circuit (PIC) that is light-sensitive

Art Unit: 2831

having storage capabilities (col 34 lines 6-10) in correcting a wavelength dependent output signal of the light sensitive integrated circuit (col 21 line 61-65, see also the correction done in figures 17 and 23), wherein the storage correction data corrects the wavelength dependent output signal (col 21 lines 61-65, see also the correction done in figure 17 and 23) and discloses wherein the system includes a temperature monitor, wherein temperature and light intensity are both related to the wavelength (col 4 lines 44-49).

Kish et al. lacks specifically a temperature sensor for measuring temperature of light source and correction data derived from the temperature so that the output signal correcting information is based on the temperature of the external light source, so that the temperatures sensor is on the integrated circuit, and wherein the integrated circuit comprises a storage medium that stores the correction data, the storage medium comprising at least one of a Zener diode, a fuse, or an EEPROM.

Kai et al. discloses a temperature sensor that determines a temperature of the light sources, and uses the output of the temperature sensor to control the oscillation wavelengths by compensation for temperature conditions (abstract), temperature sensor (figure 3 element 24) is in the vicinity of the LD array chip-20 (chips are known to be located on integrated circuits/wafers- there would be a type of board/motherboard/integrated circuit supporting and providing proper connections- power and ground- to the chip and thermistor, possibly being shown in the figure by the unlabeled box surrounding elements 20 and 24).

Art Unit: 2831

At the time the invention was made it would have been obvious for one of ordinary skill in the art to modify Kish et al. by adding a temperature sensor (which would be obvious to be on the integrated circuit as the PIC has optic components-abstract, and the temperature sensor would have the added functionality to make sure all the other chips on the integrated circuit and wafer don't overheat) for measuring the temperature of light source for correction of the wavelengths as taught by Kai et al., (during modification it would be known to be place on the integrated circuit of Kish et al., (similar to how Kai is described as an integrated circuit above) as the PIC -located on a wafer- has optic components-abstract- also the temperature sensor would provide the added functionality to make sure all the other chips on the integrated circuit and wafer don't overheat) in order to be able to easily control the wavelength in the system (page 1 paragraph 10).

D'Angelo discloses an integrated circuit device comprising either EPROM or EEPROM, showing they are interchangeable with zener diodes, and that they are all integrated on a circuit (col 11 lines 19-29).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Kish et al. to include an EEPROM or zenor diode in an integral system for easy storage as taught by D'Angelo in order to take up less space on the integrated circuit; also see MPEP 2144.04 V B, which combined with the reasoning that it is well known in the art to make integral all these small components on an integrated chip makes obvious the storage medium on the integrated circuit.

In regard to claim 14, Kish et al. discloses wherein the integrated circuit is on a semiconductor substrate 32 (Fig. 6).

In regard to claim 15, Kish et al. discloses wherein the integrated circuit comprises one or more photodiodes able to receive different wavelengths of light PD (Fig. 37).

In regard to claim 23, Kish et al. as modified discloses wherein the storage medium is for permanently storing information (EEPROMs and zener diodes are known in the art to be able to permanently store information- D'Angelo col 3 lines 38-42 – will not be erased after a certain amount of time or loss of power).

5. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kish et al. (7043109), Kai et al. (US Publication 2002/0070359), and D'Angelo (6621284) as applied to claim 8 above, and further in view of Schmeizer (US Publication 2002/0048022).

In regard to claim 19, Kish et al. as modified discloses wherein the integrated circuit (PIC) has a sensitivity that is wavelength dependent (i.e. the integrated circuit is sensitive to different wavelengths of laser).

Kish et al. as modified lacks wherein the measured values define a sensitivity curve, wherein a smallest interval between two of the different wavelengths on the sensitivity curve is smaller than an interval between a relative maximum and a relative minimum on the sensitivity curve, in part, by the two measured wavelengths.

Art Unit: 2831

Schmeizer et al. discloses a sensitivity curve (figure 2) based on measured values of wavelengths from LEDs or lasers (page 3 paragraph 21), wherein a smallest interval between two of the different wavelengths on the sensitivity curve is smaller than an interval between a relative maximum and a relative minimum on the sensitivity curve (figure 2, many samples are taken so intervals between wavelengths are small).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Kish et al. as modified to include a sensitivity curve using with many measurements, so that a smallest interval between two of the different wavelengths on the sensitivity curve is smaller than an interval between a relative maximum and a relative minimum on the sensitivity curve, as taught by Schmeizer et al. in order to measure the quality of dispersion or distribution of the measured values in a matrix (page 1 paragraph 4).

Allowable Subject Matter

6. Claims 1, 5-7, 17, and 20-22 are allowed.

In regard to claim 1, the prior art does not teach or render obvious the method including the combination wherein testing needles form contacts between the testing card and the integrated circuit, and wherein the testing needles are for placement on contact areas of the integrated circuit for storing data on the integrated circuit and wherein the different wavelengths of light are applied via light-emitting diodes that are mounted atop the testing card and in the combination as claimed.

Art Unit: 2831

Claims 5-7, 17, and 20-22 further limit allowable claim 1, and, therefore, are also allowable.

Response to Arguments

7. Applicant's arguments with respect to claims 8, 14, 15, 18, and 23 have been considered but are moot in view of the new ground(s) of rejection.

In regard to claim 10, applicant correctly states that Kai does not disclose or suggest that the output signal of an integrated circuit comprising a photodiode is corrected, so that the sensitivity of the photodiode would also not be included in Kai. These limitations are disclosed in Kish et al. (as described in the new rejection above), therefore the combination of Kish et al. as modified by Kai, discloses all the limitations of the currently amended claim. Because claim 10 is properly rejected, dependent claims 12, 13, and 19, remain rejected.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JEFF NATALINI whose telephone number is (571)272-2266. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on 571-272-2245. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2831

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jeff Natalini/
Examiner, Art Unit 2831